REMARKS

Claims 1-14 and 29-37 are all the claims pending in the application. Claims 1-14 stand rejected on prior art grounds. Claims 15-28 have been canceled without prejudice or disclaimer and claims 29-37 have been added. Applicants respectfully traverse the rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 5-6, 8, and 12-13 stand rejected under 35 U.S.C. §102(e) as being anticipated by She, et al., (U.S. Publication No. 2005/0242391), hereinafter referred to as She. Claims 1-7 and 15-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hsu, et al., (U.S. Patent No. 6,107,141), hereinafter referred to as Hsu. Claims 2 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hsu.

The claimed invention provides a multiple-gate transistor comprising a logic gate, a floating gate, and a programming gate. In the rejection, the Office Action argues that She discloses a floating gate; however, She discloses a trapping layer that functions as a nitride trap storage site, not as a floating gate. In addition, the Office Action argues that Hsu discloses a logic gate, a floating gate, and a programming gate. However, neither of the three gates in Hsu are adjacent a first side of the channel region (i.e., the region between the drain and source); and, neither of the three gates are adjacent a second side of the channel region, wherein the first side is opposite the second side. Rather, all three gates of Hsu are formed on the same surface of the channel region; they are all directly

over the channel region. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach the claimed invention.

The Office Action argues that She discloses a floating gate (Office Action, p. 4, para. 1, first sentence). More specifically, referencing figures 10 and 11 of She, the Office Action argues that the trapping layer (where Bit 1 and Bit 2 are trapped) is analogous to the floating gate of the claimed invention.

Applicants respectfully disagree with such a conclusion. The trapping layer of She functions as a nitride trap storage site, not as a floating gate. Specifically, as discussed in paragraph 0028 of She, the nitride layer is etched back to form two spacers 24 and 26, which are the nitride charge trap storage sites. The nitride charge trap layer is not continuous anymore. Hence the lateral migration of the charged electrons is eliminated. Therefore, contrary to the position taken in the Office Action, the trapping layer of She is a nitride trap storage site and not a floating gate.

In addition, as described in paragraph 0035 of She, and as shown in FIG. 10, the front gate (gate 1) and the back gate (gate 2) control the front side and the backside of the channel, respectively. There are source storage bit and drain storage bit ***(two bits/gate)*** associated with each gate, hence a total of 4 physical bit/cell is realized with the above structure. Therefore, the two source storage bit and drain storage bit regions are each associated with a gate (i.e., gate 1 and gate 2). Thus, Bit1 and Bit 2 cannot be a transistor gate if She explicitly teaches that they are bits that are associated with a gate.

Accordingly, contrary to the position taken in the Office Action, Applicants submit that the trapping layer (including Bit 1 and Bit 2) is not a transistor gate. As such,

it is Applicants' position that She does not teach the claimed feature of "A multiple-gate transistor comprising ... a floating gate" as defined by independent claims 1, 8, 29, and 34.

In addition, the Office Action argues that Hsu teaches a logic gate adjacent a first side of a channel region, a floating gate adjacent a second side of the channel region, and a programming gate adjacent the floating gate (Office Action, p. 5, para. 4). Specifically, the Office Action asserts that the select gate 120, the floating gate 130, and the control gate 140 of Hsu are analogous to the logic gate, floating gate, and programming gate of the claimed invention.

However, as illustrated in figure 1 of Hsu, neither of the three gates are adjacent a first side of the channel region (i.e., the region between drain 20 and source 30); and, neither of the three gates are adjacent a second side of the channel region, wherein the first side is opposite the second side. Moreover, none of the gates in Hsu are on a first side of the channel region that is opposite a gate that is a second side of the channel region. Rather, all three gates of Hsu are formed on the same surface of the channel region; they are all ***directly over*** the channel region.

Conversely, as illustrated in figure 15 of the claimed invention, the logic gate 130 is adjacent a first side of the channel region 142, the floating gate 30 is adjacent a second side of the channel region 142, and the programming gate 70 is adjacent the floating gate 30.

In Hsu, neither the select gate 120, the floating gate 130, and/or the control gate 140 are adjacent a first side and/or second side of the channel region. Therefore, it is

Applicants' position that Hsu does not teach the claimed feature of "a logic gate adjacent a first side of said channel region ... a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side ... and a programming gate adjacent said floating gate" as defined by independent claims 1, 29, and 34. Furthermore, it is Applicants' position that Hsu does not teach the claimed feature of "a gate oxide on a first side of said channel region; a logic gate adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region; a first insulator on a second side of said channel region, wherein said second side of said channel region is opposite said first side; a floating gate adjacent said first insulator, wherein said first insulator is between said floating gate and said channel region; a second insulator adjacent said floating gate; and a programming gate adjacent said second insulator, wherein said second insulator is between said programming gate and said floating gate" as defined by independent claim 8.

Therefore, it is Applicants' position that neither She nor Hsu teach many features defined by independent claims 1, 8, 29, and 34; and, that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-14, 30-33, and 35-37 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

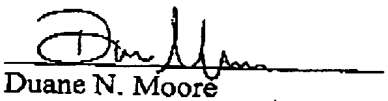
II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-14 and 29-37, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 6/1/06



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